The list of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Original) A method for driving a first wordline in a semiconductor memory device having a mode register, the method comprising:

generating a wordline drive signal for activating the first wordline in response to a drive signal; and

generating a wordline reset signal for deactivating the first wordline in response to the drive signal, a refresh wordline signal established during a refresh operation, and a mode register set wordline signal provided from the mode register.

2. (Original) The method of Claim 1, wherein the first wordline is one of a plurality of wordlines included in the semiconductor memory device, and wherein the mode register set wordline signal is used to screen for defective wordlines in the plurality of wordlines.

3. (Original) The method of Claim 1, further comprising generating a delayed version of a master refresh signal, and wherein the refresh wordline signal is generated in response to the delayed master refresh signal.

4. (Original) The method of Claim 3, further comprising:

generating an oscillation signal in response to the master refresh signal;

generating a pulsed refresh signal from the oscillation signal;

generating a refresh start signal in response to the pulsed refresh signal and the delayed refresh master signal; and

generating the refresh wordline signal in response to both the delayed refresh master signal and the refresh start signal.

5. (Original) The method of Claim 4, wherein generating the pulsed refresh signal from the oscillation signal comprises converting the oscillation signal into a frequency-demultiplied signal and generating the pulsed refresh signal from the frequency-demultiplied signal.

6. (Original) A semiconductor memory device comprising:

a wordline;

a bitline;

a memory cell coupled to the wordline and the bitline;

a mode register;

a wordline driver for activating the wordline to access data stored in the memory cell in response to a wordline drive signal, a wordline reset signal, and a wordline enable signal; and

a wordline drive controller configured to generate the wordline drive signal and the wordline reset signal in response to a main drive signal, a refresh wordline signal established during a refresh operation, and a mode register set wordline signal provided from the mode register.

7. (Original) The semiconductor memory device of Claim 6, further comprising a refresh wordline controller that generates the refresh wordline signal in response to a master refresh signal.

8. (Original) The semiconductor memory device of Claim 7, wherein the refresh wordline controller comprises:

a pulsed refresh signal generation circuit that is configured to generates a pulsed refresh signal from an oscillation signal;

a refresh start signal generation circuit that is configured to generate a refresh start signal in response to the pulsed refresh signal and a delayed version of the master refresh signal; and

a circuit configured to generate the refresh wordline signal in response to the delayed master refresh signal and the refresh start signal.

9. (Original) The semiconductor memory device of Claim 6, wherein the wordline driver includes a transistor which connects the wordline to a ground voltage in response to the wordline reset signal.

10. (Original) The semiconductor memory device of Claim 9, wherein the refresh wordline signal controls activation of the wordline reset signal during the refresh operation of the device.

11. (Original) The semiconductor memory device of Claim 9, wherein the mode register set wordline signal controls activation of the wordline reset signal during a test operation of the device that screens the wordline to determine if the wordline is defective.

12. (Original) The semiconductor memory device of Claim 6, wherein the main drive signal is derived from a row address signal.

13. (Original) The semiconductor memory device of Claim 6, wherein the wordline drive controller comprises a circuit that generates the wordline reset signal as a logical NOR operation of the drive signal and a second signal that comprises the output of a logical OR operation of the refresh wordline signal and the mode register set wordline signal.

14. (Original) The semiconductor memory device of Claim 8, wherein the circuit configured to generate the refresh wordline signal in response to the delayed master refresh signal and the refresh start signal performs a logical NOR operation on at least the inverse of the self refresh master signal and the self refresh start signal.

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Cancelled)

20. (Cancelled).

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)